Application No. 10/815,431
Amendment dated January 27, 2006
Response to Office Action of October 27, 2005

Atty. Docket No. 42P17830
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TC/A.U. 2112

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1.   (Currently Amended) A method comprising:

receiving an interrupt message from a device via a shared interrupt interface;

checking one or more <u>status</u> registers to identify the device; and

transmitting an indication of the interrupt message to one or more selected operating entities <u>associated with</u> based on the identity of the <u>identified</u> device.

2.   (Original) The method of claim 1 wherein the one or more selected operating entities comprises one or more virtual machines.

3.   (Original) The method of claim 1 wherein the one or more selected operating entities comprises threads in a multi-threaded operating environment.

4.   (Original) The method of claim 1 wherein the one or more registers comprise at least one Peripheral Component Interconnect (PCI) Status register for one or more corresponding devices.

5.   (Original) The method of claim 4 wherein the PCI Status register conforms to the PCI Bus Standard, Version 2.3 or higher.

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6.   (Original) The method of claim 4 wherein the PCI Status register conforms to the PCI Express Bus Standard, Version 1.0 or higher.

7.   (Currently Amended) The method of claim 1 wherein the one or more operating entities ~~virtual machines~~ comprise virtual machines [[that]] registered to have access to the identified device.

8.   (Currently Amended) The method of claim 1 further comprising executing an interrupt service routine chain with each of the one or more ~~virtual machines~~ operating entities.

9.   (Original) The method of claim 1 wherein the shared interrupt interface comprises a bus that conforms to a Peripheral Component Interconnect (PCI) standard.

10.   (Currently Amended) The method of claim 1 wherein transmitting an indication of the interrupt message to one or more operating entities ~~virtual machines~~ based on the identity of the device comprises transmitting an identity of the device.

11.   (Currently Amended) An article comprising a computer-accessible medium having stored thereon instructions that, when executed, cause one or more processors to:

receive an interrupt message from a device via a shared interrupt interface;

check one or more status registers to identify the device; and

transmit an indication of the interrupt message to one or more selected operating

entities associated with based on the identity of the identified device.

12.   (Original) The article of claim 11 wherein the one or more selected

operating entities comprises one or more virtual machines.

13.   (Original) The article of claim 11 wherein the one or more selected

operating entities comprises threads in a multi-threaded operating environment.

14.   (Original) The article of claim 11 wherein the one or more registers

comprise at least one Peripheral Component Interconnect (PCI) Status register for one or

more corresponding devices.

15.   (Original) The article of claim 14 wherein the PCI Status register

conforms to the PCI Bus Standard, Version 2.3 or higher.

16.   (Original) The article of claim 14 wherein the PCI Status register

conforms to the PCI Express Bus Standard, Version 1.0 or higher.

17.   (Currently Amended) The article of claim 11 wherein the one or more

operating entities ~~virtual machines~~ comprise virtual machines that registered to have

access to the identified device.

18.   (Currently Amended) The article of claim 11 further comprising

instructions that, when executed cause the one or more processors to execute an interrupt

service routine chain with each of the one or more ~~virtual machines~~ operating entities.

19.   (Original) The article of claim 11 wherein the shared interrupt interface

comprises a bus that conforms to a Peripheral Component Interconnect (PCI) standard.

20.   (Original) The article of claim 11 wherein the instructions that cause the

one or more processors to transmit an indication of the interrupt message to one or more

operating entities ~~virtual machines~~ based on the identity of the device comprise

instructions that, when executed, cause the one or more processors to transmit an identity

of the device.

21.   (Currently Amended) An apparatus comprising:

a plurality of virtual machines having associated respective operating systems;

a host monitor communicatively coupled with the plurality of virtual machines

and coupled to receive an interrupt signal via a shared interrupt interface, wherein the

host monitor reads a value stored in one or more status registers corresponding to devices

that asserted the interrupt signal to identify the device, and further wherein the host

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monitor selectively invokes an interrupt service signal to each of the plurality of virtual

machines associated with the device asserting the interrupt signal.

22.   (Original) The apparatus of claim 21 wherein the one or more registers

comprise at least one Peripheral Component Interconnect (PCI) Status register for one or

more corresponding devices.

23.   (Original) The apparatus of claim 22 wherein the PCI Status register

conforms to the PCI Bus Standard, Version 2.3 or higher.

24.   (Original) The apparatus of claim 22 wherein the PCI Status register

conforms to the PCI Express Bus Standard, Version 1.0 or higher.

25.   (Original) The apparatus of claim 21 wherein each virtual machine

receiving the interrupt service signal from the host monitor executes at least one interrupt

service routine.

26.   (Original) The apparatus of claim 21 wherein the shared interrupt

interface comprises a bus that conforms to a Peripheral Component Interconnect (PCI)

standard.

27.   (Original) The apparatus of claim 21 wherein the interrupt service signal

comprises an identifier of the device.

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28.   (Currently Amended) A system comprising:

a memory controller; and

an article communicatively coupled with the memory controller, the article

comprising a computer-accessible medium having stored thereon instructions that, when

executed, cause one or more processors to receive an interrupt message from a device via

a shared interrupt interface, check one or more status registers to identify the device, and

transmit an indication of the interrupt message to one or more operating entities

associated with based on the identity of the identified device.

29.   (Original) The system of claim 28 wherein the one or more selected

operating entities comprises one or more virtual machines.

30.   (Original) The system of claim 28 wherein the one or more selected

operating entities comprises threads in a multi-threaded operating environment.

31.   (Original) The system of claim 28 wherein the one or more registers

comprise at least one Peripheral Component Interconnect (PCI) Status register for one or

more corresponding devices.

32.   (Original) The system of claim 31 wherein the PCI Status register

conforms to the PCI Bus Standard, Version 2.3 or higher.

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33.   (Original) The system of claim 31 wherein the PCI Status register conforms to the PCI Express Bus Standard, Version 1.0 or higher.

34.   (Currently Amended) The system of claim 28 further comprising instructions that, when executed cause the one or more processors to execute an interrupt service routine chain with each of the one or more ~~virtual machines~~ <u>operating entities</u>.

35.   (Original) The system of claim 28 wherein the shared interrupt interface comprises a bus that conforms to a Peripheral Component Interconnect (PCI) standard.